

## Asymptotic notation review I

Asymptotic analysis gives us a means of speaking of arbitrarily large growth, independently of arbitrarily (but finitely) large costs not associated with problem size.

| Notation | Name | Definition | Introduced |
| :--- | :--- | :--- | :--- |
| $f(n) \in \mathcal{O}(g(n))$ | Big O | $\exists k>0, \exists n_{0}, \forall n$ | Paul Bachmann |
|  |  | $n>n_{0} \Longrightarrow f(n) \leq g(n) * k$ | $(1894)$ |
| $f(n) \in o(g(n))$ | Small O | $\forall k>0, \exists n_{0}, \forall n$ |  |
|  |  | $n>n_{0} \Longrightarrow\|f(n)\| \leq\|g(n)\| * k$ | Edmund Landau |
|  |  | $(1909)$ |  |
| $f(n) \in \Theta(g(n))$ | Big Theta | $\exists k_{1}>0, \exists k_{2}>0, \exists n_{0}, \forall n$ | Donald Knuth |
|  |  | $n>n_{0} \Longrightarrow g(n) * k_{1} \leq f(n)$, | $(1976)$ |
|  |  | $f(n) \leq g(n) * k_{2}$ |  |
| $f(n) \in \omega(g(n))$ | Small Omega | $\forall k>0, \exists n_{0}, \forall n$ | Donald Knuth |
|  |  | $n>n_{0} \Longrightarrow\|f(n)\| \geq\|g(n)\| * k$ | (1976) |
| $f(n) \in \Omega(g(n))$ | Big Omega | $\exists k>0, \exists n_{0}, \forall n$ |  |
|  |  | $n>n_{0} \Longrightarrow f(n)>g(n) * k$ | Donald Knuth <br> (1976) |

Advances in (finite) computing technology can only reduce these ignored costs.
Wrap the earth with your register file, and still there will be numbers so large that their addition is $\Theta(n)$.

## Asymptotic notation review II

| Class (all $\left.c_{*}>1\right)$ | Name | Example |
| :--- | :--- | :--- |
| $\mathcal{O}(1)$ | Constant | Is word-sized unsigned int $n$ a power of 2? |
| $\mathcal{O}\left(\lg _{c_{1}} \lg _{c_{2}} n\right)$ | Double-log | Interpolative search on uniform distribution |
| $\mathcal{O}\left(\lg _{c} n\right)$ | Logarithmic | Binary search |
| $\mathcal{O}(n \lg n)=\mathcal{O}(\lg n!)$ | Linearithmic | FFT |
| $\mathcal{O}\left(n^{c}\right)$ | Polynomial | Primality testing |
| $\mathcal{O}\left(c^{n}\right)$ | Exponential | Brute-force Boolean equivalence |
| $\mathcal{O}(n!)$ | Factorial | Unrestricted permutations of a poset |
| $\mathcal{O}\left(c_{1}^{c_{2}^{n}}\right)$ | Double-exp | Presburger arithmetic decision best case |

Speaking of still faster growth rates ${ }^{1}$ (hyper-exponential, $\mathcal{A}$ ) is mostly zoology.
${ }^{1}$ Check out "fast-growing hierarchies" and the LöbWainer hierarchy.

## It's the constants, stupid

Algorithmic choices can dominate performance, especially at scale. By the definition of Big O, it should also be obvious that an asymptotically superior algorithm can be slower for small inputs ${ }^{2}$.

That said, no one's going to think implementing a routing table with a linked list is a good idea.

Furthermore, asymptotic analysis speaks of performance as problem size grows. It doesn't speak of real-time. It doesn't speak of bounded memories. We rarely speak of piecewise asymptotics.

But, by all means, do ensure you're not doing linear searches on sorted data etc.

[^0]
## What's hiding behind $\mathcal{O}$ ?

Naive square ( $n \mathrm{Xn} \mathrm{X} n \mathrm{Xn}$ ) matrix multiplication is $\Theta\left(n^{3}\right)$.

$$
\begin{equation*}
C=A B \Longrightarrow C_{i j}=\sum_{m=1}^{k} A_{i m} B_{m j} \tag{1}
\end{equation*}
$$

Counting the explicit additions and multiplications, there are precisely $2 n^{3}$ "operations".

## Fused multiply-add

IEEE 754-2008 floating point support requires FMA, fused multiply-add. Let $r n()$ denote a rounding operation. Typically, a multiply-add chain requires two instructions, and rounds twice:

$$
\begin{equation*}
M A C(A, B, C)=r n(r n(A * B)+C) \tag{2}
\end{equation*}
$$

Fused multiply-add rounds only once, preserving the fully precise product in an internal register:

$$
\begin{equation*}
F M A(A, B, C)=r n(A * B+C) \tag{3}
\end{equation*}
$$

AMD's FMA4 (Bulldozer) implements a fully general SIMD FP FMA. Intel's FMA3 (Haswell, as part of AVX2; also in AMD's Piledriver) implements a destructive SIMD FP FMA ${ }^{3}$. The throughput and latency are equivalent to standard single SIMD FP adds and multiplies. NVIDIA's Fermi likewise introduced a full-throughput FMA.

There are now precisely $n^{3}$ "operations".
${ }^{3}$ AMD's XOP further implements an SIMD integer FMA.

## Wide issue



Haswell can issue and retire 2 VFMADD* instructions per cycle.
There are now precisely $n^{3} / 2$ "operations" ${ }^{4}$.
${ }^{4}$ Assuming that two operations are available every cycle.

| 0.0 | xmm0 |
| :---: | :---: |
| ymm0 |  |
| 0.0 | xmm1 |
| ymm1 |  |
| . . | . . |
| . . |  |
| 0.0 | xmm14 |
| ymm14 |  |
| 0.0 | xmm15 |
| ymm15 |  |

AVX uses the 16 256-bit YMM registers. There are 8 32-bit IEEE 754-2008 single-precision values in a 256 -bit input.
There are now precisely $n^{3} / 16$ "operations" ${ }^{5}$.
${ }^{5}$ Assuming that values are usable in 256-bit chunks.

## Multicore



Haswell will likely debut in a quadcore physical package.
There are now precisely $n^{3} / 64$ "operations" ${ }^{a}$.
${ }^{a}$ Ignoring communication costs, and assuming perfect parallelism.

## Memory accesses

(1) $\forall i, 0 \leq i \leq n$ : Read row $i$ from $A$ into $a$
(2) $\forall j, 0 \leq j \leq n$ : Read column $j$ from $B$ into $b$, read $C_{i j}$ into $c$
(3) $\forall k, 0 \leq k \leq n$ : Store $a_{k} * b_{k}+c$ into $C_{i j}$
(1) $n^{2}$ loads from A
(2) $n^{3}$ loads from B
(3) $n^{2}$ loads from C
(1) $n^{2}$ stores to C

Counting the loads and stores, there are precisely $n^{3}+3 n^{2}$ memory accesses. There are now precisely $\frac{65 n^{3}}{64}+3 n^{2}$ "operations".

Arithmetic intensity

$$
\lim _{n \rightarrow \infty} \frac{\text { Arithmetic }}{\text { Memory }}=2
$$

## Loads and stores

Hong and Kung proved in 1981 that any schedule of conventional matrix multiplication must transfer $\Omega\left(\frac{n^{3}}{\sqrt{Z}}\right), Z<\frac{n^{2}}{6}$ words between slow and fast memory. Tiling is the optimal strategy.

Of course, AVX's VMOVAPS moves 256 bits, or 832 -bit single precision floating point words, at a time. And there's 4 cores. With two load/store pipes each. So that's $\Omega_{H K} / 64^{6}$.

Of course, we're not going to be able to pack two VFMADDPS and two VMOVAPS instructions into every $16 \mathrm{~B} / \mathrm{c}$ I $\$$ fetch ${ }^{7}$.

How does this interact with register banking? Multilevel caching? TLBs? Page cache? Prefetching? DRAM banking? Multilevel disk? Logical cores? Other physical cores? NUMA?

[^1]
## Argh



## CS4803 Spring 2010 Lab 3-All $\mathcal{O}\left(n^{3}\right)$

Core 2 Duo 6600 ( 2.4 GHz ) + GeForce 8400 GS G98 PCI ( 567 MHz )


## ATLAS Unleashed-All $\mathcal{O}\left(n^{3}\right)$

Iterative, Iterative, Mini, ATLAS, Unleashed, 168 Iterative, Iterative Mini, ATLAS, CGwS, 44 Iterative, Iterative, Mini, Coloring, BRILA, 120 Iterative, Iterative, Micro, Coloring, BRILA, 120 Recursive, Iterative, Mini, ATLAS, Unleashed, 168

Recursive, Iterative, Mini, ATLAS, CGwS, 44 Recursive, Iterative, Mini, Coloring, BRILA, 120 Recursive, Iterative, Micro, Coloring, BRILA, 120 Recursive, Recursive, Micro, Coloring, BRILA, 8 Recursive, Recursive, Micro, Belady, BRILA 8 Recursive, Recursive, Micro, Scalarized, Compiler, 4

Recursive, Recursive, Micro, None, Compiler, 12 Iterative, Statement, None, None, Compiler, 1 Recursive, Recursive, Micro, None, Compiler, $1 \cdots$-...

## Outer Control Structure



Ultrasparc Illi


In the pure systems space, $\mathcal{O}$ makes still less sense. What's $\mathcal{O}$ of multithreaded file lexing?


Core i7 2600 K (all data sets fit in memory)

Nonetheless, optimization can be very fruitful.


## Analysis-driven optimization I

```
samples pont kernel function
```

```
12022.00 - 44.9% : read_hpet
1766.00 - 6.6% : spin_lock_irqsave
1269.00 - 4.7% : acpi_os_read_port
1209.00 - 4.5% : hpet_next_event
    410.00 - 1.5% : schedule
    280.00 - 1.0% : do_sys_poll
    273.00 - 1.0% : sched_clock_local
    265.00 - 1.0% : fget_light
    241.00 - 0.9% : native_read_tsc
    237.00 - 0.9% : _spin_lock
    231.00 - 0.9% : spin unlock irgrestore
```

High-level ("Macroanalysis")
Coarse tools and algorithmic reasoning, e.g.:

- Ensure sufficient task-level parallelism
- Ensure cores aren't overutilized
- Profiler-driven hotspot location
- High-level memory and I/O flow


## Analysis-driven optimization II



Low-level ("Microanalysis")

## Timelin

Multipri

Kernel I
Kernel I

Performance counters and throughput-based reasoning, e.g.:

- Vectorize
- Tune for caches
- Watch for $\mu$ architectural stalls


## Complexity finds a way




3 Iterations


4 Iterations

A fractal having Hausdorff dimension 2,
the space-filling Peano curve is used in cache-oblivious algorithms.
Mastering the complex modern design space requires deftly switching between theoretical analysis, guided experiment, and pure exploration.

This class is about doing so.


Insert $2 / 3$


## Insert $3 / 3$



## Recommended reading

- Hong and Kung. "I/O complexity: The red-blue pebble game" (1981).
- Yotov et al. "An experimental comparison of cache-oblivious and cache-conscious programs" (2007).
- Irony et al. "Communication Lower Bounds for Distributed-Memory Matrix Mul" (2004).
- Goto et al. "Anatomy of High-Performance Matrix Multiplication" (2008).
- Kalyanasundaram et al. "Improved Simulation of NTMs" (2011).
- François Le Gall. "Faster Algorithms for Rectangular Matrix Multiplication" (2012).
- Eric Quinnell. "Floating-Point Fused Multiply-Add Architectures" (2007).
- Tom Leighton. "Better Master Theorems for Divide-and-Conquer Recurrences" (1996).
- Intel Instruction Set Extensions Programming Reference


[^0]:    ${ }^{2}$ We will see that small inputs can be surprisingly large.

[^1]:    ${ }^{6}$ Assuming that the values are located in aligned, contiguous 256 -bite chunks in memory. Wait... we can use VMOVUPS if they're unsuitably aligned.
    ${ }^{7}$ VEX-encoded VMOVAPS tends to run ${ }^{\sim} 5$ bytes.

