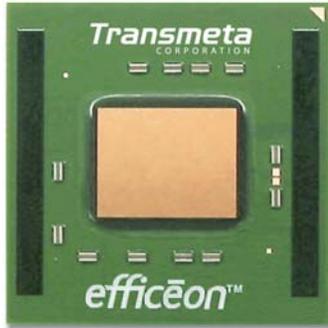# Transmeta™ Efficeon™ TM8300/TM8600 Processor

Efficeon™ Processor Model TM8300/TM8600 Features

- Advanced 256-bit VLIW processor / Code Morphing™ software x86-compatible mobile platform solution

- Leading edge 0.13µm fabrication technology for GHz performance at very low power levels

- Standard product speeds of 900 MHz - 1.2 GHz

- 128 KByte L1 instruction cache, 64 KByte L1 data cache, and 512 KByte (TM8300) or 1024 KByte (TM8600) L2 write-back cache

- SSE, SSE2, and MMX instruction support
- Integrated northbridge core logic features facilitate compact system designs
    - DDR memory controller with 100-166 MHz, 2.5 V interface
    - AGP 1x/2x/4x 1.5 V graphics interface
    - HyperTransport™ 200/400 MHz 1.2 V southbridge interface

- Enhanced LongRun™ power management with ultra-low-power operation extends battery life
    - Operates over 0.65-1.40 V core voltage range
    - Fully controlled by Code Morphing software without the need for BIOS intervention

- Enhanced LongRun thermal management dynamically adapts to system thermal environment
    - Improved dynamic control over power consumption based on work load demands
    - On-chip thermal diode for adaptive thermal control

- Full system management mode (SMM) support
- Compact 783-contact organic BGA package with 1 mm ball pitch

The Efficeon TM8300/TM8600 processor is a high-performance and low-power microprocessor, based on an advanced next-generation VLIW core architecture. When combined with Transmeta's Code Morphing software, the TM8300/TM8600 processor provides extremely high-performance x86-compatible code execution. The TM8300/TM8600 processor delivers a highly integrated, cost-effective platform solution, incorporating a large 512 Kbyte (TM8300) or 1024 KByte (TM8600) L2 cache, support for double data rate (DDR) SDRAM, and a HyperTransport I/O controller.The very low 0.65-1.40 V operating voltage of the TM8300/TM8600 processor core, in combination with Code Morphing software advanced power and thermal management capabilities, make the TM8300/TM8600 an ideal processor solution for mobile PC applications. The TM8300/TM8600 processor can operate below 1 Watt while running mobile applications.

Architecture

The Transmeta Efficeon TM8300/TM8600 processor includes a completely re-architected VLIW hardware engine and new Code Morphing software to significantly extend the advantages of Transmeta's software- based approach to x86-compatible computing. This new architecture takes even greater advantage of inherent application code parallelism, and includes additional functional units and greater VLIW instruction issue width. In combination with advanced next-generation Code Morphing software, the TM8300/TM8600 processor with a wider VLIW architecture is able to scale up efficiently in performance and frequency without the power-drain burden of complex hardware logic needed for conventional superscalar RISC and CISC architectures. Low power consumption is possible with the reduced switching logic and small die size of the VLIW architecture. With the additional device parallelism, the TM8300/TM8600 is able to accomplish more work per cycle and achieve higher core frequency operation than previous generation Transmeta processors.

Transmeta Efficeon TM8300/TM8600 Processor

In addition to the advanced 256-bit VLIW execution core, the TM8300/TM8600 processor includes SSE/ SSE2/MMX multimedia instruction support, separate 128 KByte L1 instruction and 64 KByte L1 data caches, a huge 512 KByte (TM8300) or 1024 KByte (TM8600) L2 write-back cache, a 64-bit DDR memory controller, AGP graphics bus controller, and a 8-bit HyperTransport I/O bus controller. Figure shows a block diagram of the TM8300/TM8600 processor. Integrated northbridge functions, such as the AGP and memory controllers, allow the TM8300/TM8600 processor to provide a highly integrated and cost effective platform solution for the x86 mobile PC and high-density blade server markets.

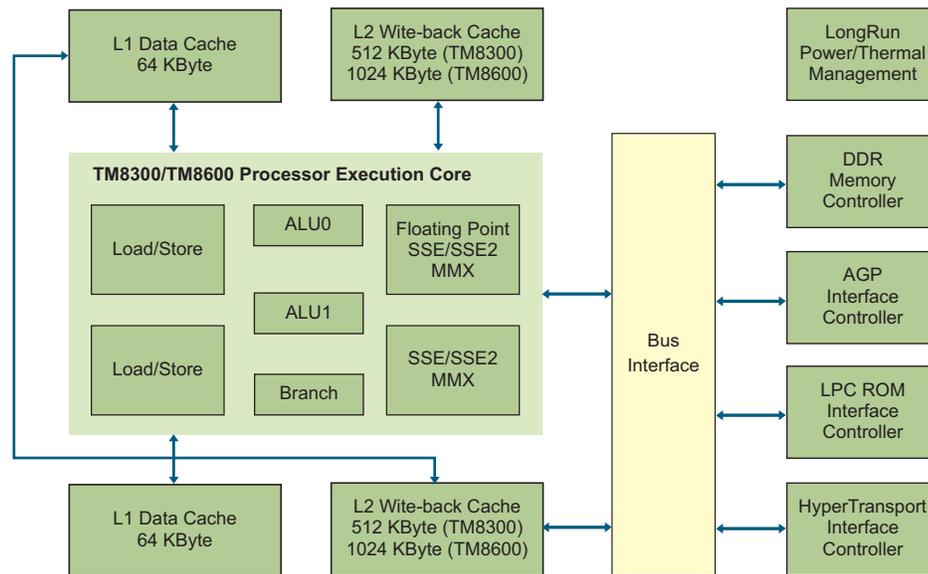**Efficeon TM8300/TM8600 Processor Block Diagram**

Figure 1

Processor Core

The Efficeon TM8300/TM8600 processor is based on a 256-bit VLIW engine with two load/store units, two integer ALU units, two multimedia SSE/SSE2/MMX units, a floating point unit, and a branch unit. A Transmeta processor long instruction word is referred to as a molecule, which is up to 256-bits long in the TM8300/ TM8600 processor. The 256-bit engine allows execution of up to seven 32-bit operations (atoms per cycle), plus a 32-bit opcode extension. During execution, molecules are packed as fully as possible to keep the processor running at full speed and all atoms within a molecule are executed in parallel. The wider 256-bit engine in the TM8300/TM8600 processor executes more atoms per cycle than previous Transmeta processors. By accomplishing more work per cycle, TM8300/TM8600 processors are more energy efficient than previous generation Transmeta processors, and significantly more energy efficient than CISC and RISC- based x86 processor architectures.

The TM8300/TM8600 processor core architecture is relatively simple by conventional standards. It is based on a VLIW 256-bit instruction set. Within this VLIW architecture, the control logic of the processor is kept very simple and software is used to control the scheduling of instructions. This allows a simplified and very straightforward hardware implementation, with an in-order 10-stage integer pipeline and a 12-stage floating point pipeline. By streamlining the processor hardware and reducing the control logic transistor count, the performance-to-power ratio (energy efficiency) can be greatly improved over traditional x86 architectures.

The TM8300/TM8600 processor includes a 128 KByte L1 instruction cache, and a 64 KByte L1 data cache. The TM8300/TM8600 processor also includes an integrated 512 KByte (TM8300) or 1024 KByte (TM8600) L2 write-back cache for improved effective memory bandwidth and enhanced performance. This cache architecture ensures maximum internal memory bandwidth for performance intensive mobile applications, while maintaining a very-low-power implementation that provides a superior performance-to-power ratio (energy efficiency) relative to previous x86 processor implementations.

In addition to having execution hardware for logical, arithmetic, shift, and floating point instructions, as in conventional processors, the TM8300/TM8600 processor uses a combination of software and hardware to offer full x86 compatibility. To ease the translation process from x86 to the core VLIW instruction set, the hardware generates the same condition codes as conventional x86 processors and operates on the same 80- bit floating point numbers. Also, the translation look-aside buffer (TLB) has the same protection bits and address mapping as x86 processors. The software component of this solution is used to emulate all other features of the x86 architecture. The software that converts x86 programs into the core VLIW instructions is called Code Morphing software. The combination of Code Morphing software and the VLIW core together acts as an x86-compatible processor solution, as shown in Figure 2.

HyperTransport Interface

The TM8300/TM8600 processor includes a HyperTransport I/O bus controller. HyperTransport is a full duplex point-to-point interface capable of delivering up to 1.6 G-byte per second of aggregate bandwidth. The interface is packet-based, and each packet can be a multiple of 4-bytes in length. After read responses or writes, data packets can be 4 to 64-bytes long.

The TM8300/TM8600 processor HyperTransport interface is 8-bits wide in each direction (transmit and receive), and operates at either 200 or 400 MHz. The interface utilizes a low-voltage differential signaling scheme operating at 1.2 V. The 8-bit HyperTransport bus is able to support up to 12 times the bandwidth of 33 Mhz 32-bit PCI.

HyperTransport Bus Topology

The HyperTransport link in a TM8300/TM8600 processor system has only two nodes, the HyperTransport (HT) unit and the HyperTransport-PCI (HT-PCI) bridge on the system southbridge. By definition, the HT unit is the host bridge on this two-node single-ended chain.

From a PCI configuration standpoint, the HyperTransport link is the logical PCI bus #0, and the external PCI bus attached to the south bridge appears as a hierarchical PCI bus behind a PCI-PCI bridge. Its PCI bus number is programmable.

HyperTransport Bus Functions

The HyperTransport bus connects the TM8300/TM8600 integrated northbridge with the system southbridge and acts as the main peripheral I/O interface for the TM8300/TM8600 processor. The bus is bidirectional and 8-bit wide in each direction. It can operate at 200 or 400 MHz. The HyperTransport unit generates and accepts HyperTransport bus transactions to and from the southbridge. This involves:

- Converting between internal bus transactions and HyperTransport transactions
- Translating between internal system address and HyperTransport address spaces
- Synchronizing between core processor and HyperTransport clock domains

Additional HyperTransport unit functions include:
- Handling external interrupts and power management events
- Supporting HyperTransport configuration space (maintained in software)
- Supporting HyperTransport protocol specifications

HyperTransport functions not supported in the TM8300/TM8600 processor include:
- Isochronous transactions - no special routing is implemented for packets with the isochronous bit set.
- Software-initiated warm reset - the host reset is connected to the TM8300/TM8600 processor RESET# pin. There is no independent HyperTransport unit reset capability, so a software-initiated HyperTransport warm reset is not possible.

Accelerated Graphics Port (AGP)

The TM8300/TM8600 processor includes an integrated accelerated graphics port (AGP) interface with 1x and 2x and 4x data transfer rates. The AGP interface provides a point-to-point link between the integrated memory controller and a graphics controller. This provides a dedicated pathway to memory for graphics, and removes graphics traffic from the HyperTransport I/O bus. The AGP bus is an expansion of the standard PCI local bus with additional sideband signals and commands. The major AGP enhancements relative to PCI include pipelined memory requests and separate address and data buses.

The TM8300/TM8600 processor integrated AGP controller is 2.0 compliant, and provides a 32-bit wide data path operating at either 66 MHz (1x mode) or double data rate 66 MHz (2x mode, using 2x strobe), or double data rate 133 MHz (4x mode, using 4x strobe). The controller can queue up to 22 outstanding AGP transactions. The TM8300/TM8600 processor, with integrated memory and AGP controllers, functions as a PCI initiator and target on the AGP bus. When the AGP bus operates in AGP mode, the graphics controller is the AGP initiator, while the TM8300/TM8600 Processor acts as the AGP target.

AGP Queues

There are two types of AGP queues, the Request Queue and the Service Queue. When an AGP request is detected, either in standard pipe mode or through the SBA mode, the request information is written to the Request Queue, which has 16 entries. The Request Queue sorts the AGP command requests based on priority and AGP bus ordering rules. When the read or write requested data is ready for transfer on the bus, the previously issued requests are moved from Request Queue to the Service Queue, which has 6 entries.The Request Queue is split up into four sub-queues:

- Low priority read queue
- High priority read queue
- Low priority write queue
- High priority write queue

The Request Queue automatically reorders high priority requests in front of low priority requests.

Virtual Memory

The system AGP graphics adapter can access an area of system memory for its use. This area of system memory is referred to as the graphics aperture. The graphics adapter views the graphics aperture as contiguous address space, while the OS allocates memory in non-contiguous blocks or pages. Similar to the processor virtual memory system, a series of page table entries translate accesses within the linear aperture address range to the appropriate pages of system memory. This mapping table is called graphics aperture relocation table (GART).

PCI Transactions on the AGP Bus

PCI transactions are identified by the active A_FRAME# signal. Performing PCI transactions on the AGP bus is preferable or necessary in some circumstances. For example, the processor configures the PCI registers of the graphics adapter. Also, if the graphics adapter must perform a memory transaction smaller than 8 bytes (the minimum AGP data size), it can do so using PCI transactions.

LPC ROM Interface

The TM8300/TM8600 processor includes a low pin count (LPC) interface to access standard LPC flash ROM devices. This interface allows high-speed access to both Code Morphing software and system BIOS code directly from the processor, and includes write and erase protection. The TM8300/TM8600 processor 5-pin LPC ROM interface operates at 33 MHz for system initialization and boot-up. The interface supports memory read and memory write as defined in LPC spec rev. 1.0, and is fully LPC 1.0 compliant.

During the boot process, Code Morphing code is uncompressed from the LPC ROM to the DDR memory. Once transferred, Code Morphing software requires a portion of the system DDR memory space. The portion of DDR memory space reserved for Code Morphing software is not visible to x86 code. This interface may also be used for in-system reprogramming and in-system BIOS and Code Morphing software upgrades.

SPD Serial Interface

The TM8300/TM8600 processor includes a 2-pin SPD serial interface to read configuration data from the DDR DIMM SPD ROM during the boot process.

JTAG Test Interface

The TM8300/TM8600 Processor provides a 5-pin JTAG interface that can be used for TM8300/TM8600 processor testing. This interface supports IEEE 1149.1, EXTEST, SAMPLE/PRELOAD, BYPASS, and HiZ instructions. The JTAG interface operates up to 100 MHz.

Clocks

The TM8300/TM8600 processor input clock (CLKIN66) is multiplied up by a programmable clock multiplier to generate appropriate processor core clock frequencies. CLKIN66 requires a clean and stable 66.6 MHz input clock signal.

The processor input clock (CLKIN66) is multiplied up by another programmable clock multiplier to generate the DDR SDRAM interface clocks (M_CLK[7:0]). The standard DDR SDRAM clock interface frequencies are 133 and 166 MHz.

The processor input clock (CLKIN66) is multiplied up by another programmable clock multiplier to generate the HyperTransport interface transmit clock. The HyperTransport bus will initialize to 200 MHz, but can be changed to operate up to 400 MHz.

The processor AGP input clock (A_CLK) is multiplied up to provide the internal clock for the AGP logic. The AGP input clock is typically set at 66.6 MHz.

The TM8300/TM8600 processor also has a 32.768 KHz suspend clock input (CLK32KHZ), used internally for a Deep Sleep timer. The logic for this timer and clock input is powered by the suspend well power supply (V_SUS).

Power Supplies and Power Status

The TM8300/TM8600 processor requires six distinct power supply sources. The processor core supply (V_CORE) operating voltage varies across the range from 0.65-1.40 V nominal, depending on the processor SKU. The core power supply voltage is set by the TM8300/TM8600 processor VRDA[4:0] signals, under Code Morphing software LongRun power management control. The VRDA signals are used to control the core power supply voltage regulator output voltage.

- The processor PLL supply (V_ANLG) operating voltage is 1.5 V nominal.
- The processor DDR interface supply (V_DDR) operating voltage is 2.5 V nominal.
- The processor AGP interface power supply (V_AGP) operating voltage is 1.5 V nominal.
- The processor HyperTransport interface power supply (V_HT) operating voltage is 1.2 V nominal.
- The processor general I/O interface power supply (V_33) operating voltage is 3.3 V nominal.
- The processor suspend well power supply (V_SUS) operating voltage is 3.3 V nominal.

There are two power status inputs on the TM8300/TM8600 processor. PWROK_CORE is driven by the system to indicate the core power supply voltage is within specified operating limits. PWROK_IO is driven by the system to indicate the other interface and I/O power supplies are within specified operating limits.

Example System

An example Efficeon TM8300/TM8600 processor system-level block diagram is shown in Figure 3.

Example Efficeon TM8300/TM8600 Processor System Block Diagram
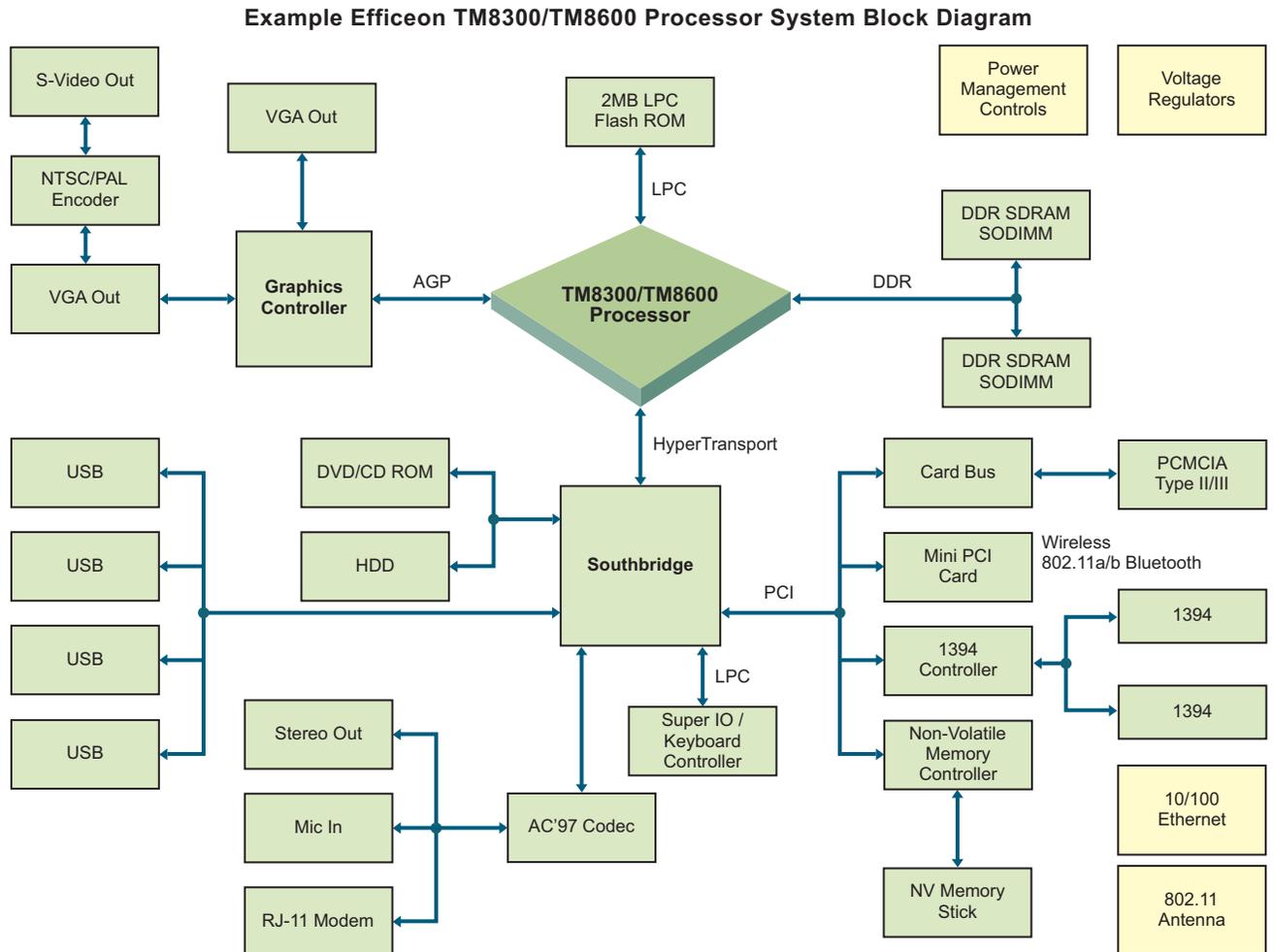

Figure 3

Power Management States

The TM8300/TM8600 processor, in conjunction with the Code Morphing software, supports ACPI-compliant power management modes. Table 1 lists the state of the TM8300/TM8600 processor for each of the ACPI global system states. The power management states listed in Table 1 are defined in greater detail in Table 2 and the following paragraphs.

System Power Management States

ACPI System State		Processor State	SDRAM State	Clock Generator State
G0 / S0 / C0	Working	Normal	Normal	Running
G0 / S0 / C1	Auto Halt	Auto Halt	Normal	Running
G0 / S0 / C2	Quick Start	Quick Start	Power saving mode	Running
G0 / S0 / C3	Deep Sleep	Deep Sleep	Self-refresh	CLKIN66 stopped
G0 / S0 / C4	Deep Sleep eXtended (DSX)	DSX	Self-refresh	CLKIN66 stopped
G1 / S1	Sleeping	Deep Sleep / DSX	Self-refresh	PLL shut down
G1 / S3	Suspend-to-RAM	Off	Self-refresh	Off
G1 / S4	Suspend-to-Disk	Off	Off	Off
G1 / S5	Soft Off	Off	Off	Off
G3	Mechanical Off	Off	Off	Off

Table 1

Processor Power Management States

Processor State	Processor Core	SDRAM	HT / AGP Controllers	Entry Trigger	Snoops	Interrupts
Normal	Running	Running	Running	Normal Operation	Serviced	Serviced
Auto Halt	Stopped	Running	Running	Executing a HLT instruction	Serviced	Serviced
Quick Start	Stopped	Power saving mode	Running	HyperTransport STPCLK assert packet with SMAF=C2	Serviced	Serviced
Deep Sleep	Stopped	Self-refresh	Stopped	HyperTransport STPCLK assert packet with SMAF=C3	Not allowed	Not allowed
DSX	Stopped	Self-refresh	Stopped	Reduce V_CORE while in Deep Sleep	Not allowed	Not Allowed

Table 2

Auto Halt

The Auto Halt state is a low-power mode entered through the execution of the HLT instruction. The Auto Halt state is exited upon an interrupt or assertion of RESET#. Snoops are serviced while in the Auto Halt state.

Quick Start

The Quick Start state is entered from the Normal and Auto Halt states when a HyperTransport STPCLK assert packet is received with the SMAF bits set for C2. The SMAF = C2 bit settings come from the ACPI BIOS. While in Quick Start, snoops are serviced and interrupts are latched. Latched interrupts are serviced once the processor returns to the Normal state. Only one occurrence of an interrupt is latched while in Quick Start. If RESET# is asserted while in Quick Start, processor initialization occurs and the processor then returns to the Normal state.

Deep Sleep

The Deep Sleep state is a very low power state the processor can enter while still maintaining its context. From the Normal and Auto Halt states, the processor enters Deep Sleep when a HyperTransport STPCLK assert package is received with the SMAF bits set for C3. The SMAF = C3 bit settings come from the ACPI BIOS. H_STOP# should be stopped at a low state when the processor enters the Deep Sleep state. The TM8300/TM8600 processor internal PLL is shut down while in Deep Sleep. When the clocks are restarted to exit Deep Sleep, the system must allow time for PLL resynchronization. Snoops are not serviced and interrupts are neither serviced nor latched while in Deep Sleep. RESET# is ignored while the processor clock signal is not toggling.

Deep Sleep Extended (DSX)

DSX is the lowest power state the processor can enter while still maintaining context. DSX is an extended Deep Sleep state with V_CORE reduced to a minimal sustaining level

LongRun Power Management

LongRun power management technology provides Code Morphing software with the ability to adjust the TM8300/TM8600 processor core operating voltage and clock frequency dynamically, depending on the demands placed on the processor by software. Because power varies linearly with clock speed and by the square of voltage, adjusting both processor voltage and clock frequency can produce cubic reductions in power consumption, whereas conventional processors can adjust power linearly only by adjusting the effective operating frequency.

The LongRun power management policies are implemented within Code Morphing software, and can detect different workload scenarios based on runtime performance information, and then exploit these by adapting processor power usage accordingly. This ensures the processor delivers high performance when necessary and conserves power when demand on the processor is low. All power adjustments are transparent to the operating system, power management controller, and the user. LongRun power management uses a number of core frequency/voltage operating points, allowing TM8300/TM8600 processors to optimize for the lowest power and maximum performance along this curve, as shown in Figure 4.

LongRun Power Management Operating Points
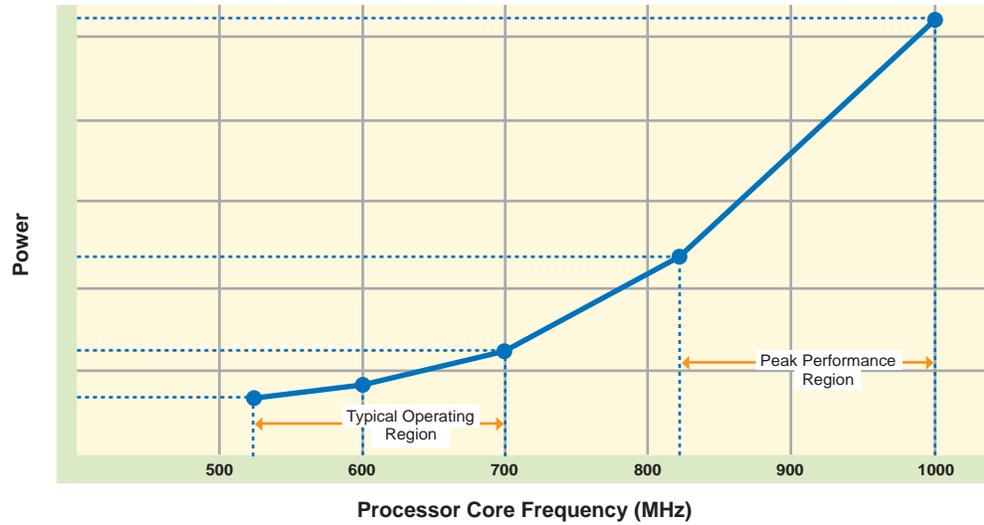
Figure 4

Most conventional x86 processors utilize ACPI policies to regulate their power consumption, the processor rapidly alternating between running at full-speed and being effectively turned off (called clock-throttling). This approach can potentially disable the processor just when a critical application needs it. In contrast, LongRun power management dynamically selects the appropriate clock speed and operating voltage needed to run the application, thereby allowing maximum energy efficiency. LongRun power management works in conjunction with ACPI. When the processor frequency and voltage scaling reaches the minimum LongRun power management setpoint, the processor transparently switches over to traditional power models, allowing policies such as ACPI to handle power management at very low power operating points.

LongRun Thermal Management

Thermal management of TM8300/TM8600 processors is integrated into the LongRun power management frequency/voltage ramp policies. The LongRun thermal management policy manages the TM8300/TM8600 processor thermal environment by using frequency/voltage shifts as a substitute for thermal throttling. In contrast to conventional thermal management techniques, LongRun thermal management delivers higher performance at the same die temperature, or the same performance at a lower die temperature. LongRun thermal management essentially expands the thermal budget of the processor. LongRun thermal management maximizes system performance and maintains safe processor operating temperatures within constrained thermal environments.

Figure 5 shows LongRun thermal management operating points for TM8300/TM8600 1000 MHz processors. Other TM8300/TM8600 processor SKUs have similar LongRun thermal operating point graphs.

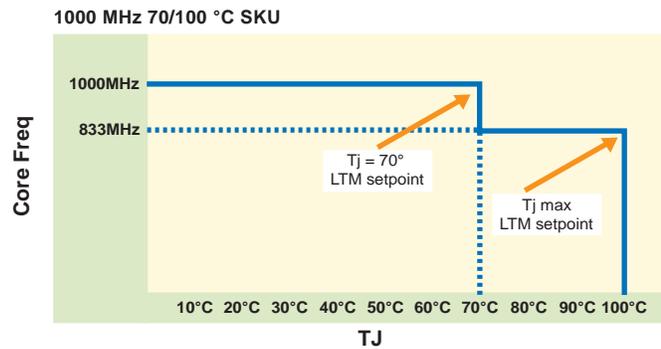**LongRun Thermal Management (LTM) Operating Curves**

1000 MHz 70/100 °C SKU

Figure 5

Typical Operating Power

Table 3 shows typical Efficeon TM8300/TM8600 processor power usage for each of the processor power management states.

Efficeon TM8300/TM8600 Processor Typical Power Usage

Application Workload	ACPI System State	ACPI System State
DVD Playback	C0-C3	1.2-2.0 W
MP3 Playback	C0-C3	0.75-0.85 W
Auto Halt	C1	0.60 W
Quickstart	C2	0.55 W
Deep Sleep	C3	170 mW
DSX	C4	75 mW

Table 3